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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/618,708	07/15/2003	Jose L. Ramos	017750-801	4909

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EXAMINER	
PAN, YUWEN	

ART UNIT	PAPER NUMBER
2618	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/618,708	RAMOS, JOSE L.	
	Examiner	Art Unit	
	YUWEN PAN	2618	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 December 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9,11 and 17-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9,11 and 17-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Response to Arguments

1. Applicant's arguments, see applicant's remarks, filed 12/10/09, with respect to the rejection(s) of claim(s) 1 under 35 USC 103 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Duffalo et al (U.S. Patent# 4,890,069, hereinafter Duffalo).

DETAILED ACTION

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claim1-9, 11, and 17 are rejected under 35 U.S.C. 112, first paragraph, as based on a disclosure which is not enabling. A capacitor that is connected between the drain of the first amplifier and the gat of the second amplifier is critical or essential to the practice of the invention, but not included in the claim(s) is not enabled by the disclosure. See *In re Mayhew*, 527 F.2d 1229, 188 USPQ 356 (CCPA 1976). The specification states that a capacitor is need to prevent any DC bias current. The examiner believes that without the involving of the capacitor the circuit is not enabled.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-5, 7, 8, and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Turlington et al (US005940031A, hereinafter Turlington) in view Khorram (U.S. US007088969B2, hereinafter Khorram) and Duffalo.

Per claim 1, Turlington discloses an apparatus (see figure 4 and 6), comprising: an antenna (see item 90, column 1 and lines 60-63); an amplifier unit connected to the antenna, a first switch that connects a transmit path of the antenna to the amplifier unit (see figure 6 and item 142); a second switch that connects a receive path of the antenna to the amplifier unit (see item 132); and a switch controller (see item 168) that is programmed to adjust positions of the first and second switches so that the amplifier unit is connected to the transmit or receive path of the antenna after a predetermined amount of time has elapsed since a prior adjustment (see column 5 and lines 52-67). Turlington does teaches that the amplifier unit includes a first amplifier and second amplifier (see figure 6 and item 126, 128, 138 140, 148 152, 154 and 156). Thurlington does not teach that the first amplifier and the second amplifier each include a source, a drain and a gate, respectively, wherein the gate of the first amplifier and the gate of the second amplifier are connected to a common gate connection, wherein the drain of the first amplifier and the drain of the second amplifier are connected to a common drain connection. Khorram teaches that an amplifier includes a plurality of transistors connected such that each amplifier has a common drain connection and a common gate connection (see figure 9, see abstract, column 10 and lines 60-column 11 and lines 25). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the references to implement a linear, multiple stage power amplifier.

Combination of Turlington and Khorram does not teach wherein the drain of the first amplifier is connected to the gat of second amplifier. Duffalo teaches such limitation (see figure 1 and items 44, 54 and 51). It would have been obvious to combine the references to properly supply DC bias current to the gate of the second amplifier.

Per claim 2, Thurlington further teaches the switch (142) with an output (b) connected to the amplifier (item 148 and 150), a first input connected to the received path (item 84 and 106) and a second input (a) connected to the transmit path (see figure 6).

Per claim 3, Thurlington further teaches a second switch (item 18), wherein the second switch (item 132) has first switch position (c) connecting a signal for transmission to the antenna, and a second switch position (b) connecting the receiving path to the antenna (see figure 6).

Per claim 4, Thurlington further teaches that a switch controller (see item 168) which controls the first and second switches to selectively connect the antenna to the amplifier for amplification of a received signal and the amplifier to the antenna for amplification of a signal for transmission (see column 5 and lines 52-67).

Per claim 5, Khorram further teaches that a third amplifier includes a source, a drain, and a gate, wherein the gate of the third amplifier is connected to the common gate connection, wherein the drain of the drain amplifier is connected to the common drain connection (see figure 9, see abstract, column 10 and lines 60-column 11 and lines 25).

Per claim 7, Thurlington further teaches that the amplifier is monolithic microwave integrated circuits (see abstract).

Per claim 8, Turlington discloses a method for transmission and reception of signals using a transceiver that includes an antenna (see figure 9 and item 90), first and second switches, and an amplifier unit for amplification of the first signal(see figure 4 and item 76, column 4 and lines 66-column5 and lines 3), the method comprising: setting the first switch (see figure 6 and item 132) to a first position, the first position connecting a signal for transmission to the amplifier unit (see item 136 and part of item 76 as in figure 6); setting the second switch to a first position, the first position connecting the amplified signal for transmission to the antenna (see item 90); setting the first switch, after the predetermined amount of time, to a second position, the second position connecting the receive path to the amplifier unit for amplification of a second signal received from the antenna(see figure 6, column 5 and lines 53-column 6 and lines 39); and setting the second switch, after a predetermined amount of time, to a second position, the second position of the second switch connecting the amplified second signal for further processing of the amplified second signal (column 5 and lines 53-column 6 and lines 39).

Turlington does teaches that the amplifier unit includes a first amplifier and second amplifier. Thurlington does not teach that the first amplifier and the second amplifier each include a source, a drain and a gate, respectively, wherein the gate of the first amplifier and the gate of the second amplifier are connected to a common gate connection, wherein the drain of the first amplifier and the drain of the second amplifier are connected to a common drain

connection. Khorram teaches that an amplifier includes a plurality of transistors connected such that each amplifier has a common drain connection and a common gate connection (see figure 9, see abstract, column 10 and lines 60-column 11 and lines 25). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the references to implement a linear, multiple stage power amplifier.

Combination of Turlington and Khorram does not teach wherein the drain of the first amplifier is connected to the gat of second amplifier. Duffalo teaches such limitation (see figure 1 and items 44, 54 and 51). It would have been obvious to combine the references to properly supply DC bias current to the gate of the second amplifier.

Per claim 9, Turlington further teaches further teaches that the second switch is in the second position the amplified signal from the receive path is connected to receiver circuitry (see figure 6, item 84, 106, and 142).

Per claim 12, Turlington discloses an apparatus comprising: an antenna (see figure 4 and item 90); an amplifier (see figure 4 and 6, item 76 and 148) connect to the antenna; a transmit path (item 86), connected to the amplifier (76), which provides a signal for amplificationi to the amplifier, and a receive path (84), connected to the amplifier (76), which receives an amplified signal from the amplifier (see column 4 and lines 36-47, column 4 lines 66-column 5 and lines 3).

6. Claims 6, 11 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Thurlington, Dufflo and Khorram as applied to claim 1 above, and further in view of Saxler (US007030428B2, hereinafter Saxler).

Per claim 6 and 17, Thurlington doesn't teach that the amplifier is fabricated in GaN-based material. Saxler teaches that High electron mobility transistors can be fabricated in the gallium nitride/aluminum gallium nitride (GaN/AlGaN) material (see column 1 and lines 63). It would have been obvious to one of the ordinary skill in the art at the time the invention was made to combine the teaching of Saxler with Thurlington's device to have the potential to generate large amounts of PF power for the power amplifier.

Per claim 11, Thurlington does not teach that the amplifier unit is an AIGaN amplifier unit. Saxler teaches that High electron mobility transistors can be fabricated in the gallium nitride/aluminum gallium nitride (GaN/AlGaN) material (see column 1 and lines 63). It would have been obvious to one of the ordinary skill in the art at the time the invention was made to combine the teaching of Saxler with Thurlington's device to have the potential to generate large amounts of PF power for the power amplifier.

7. Claims 18-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Khorram in view of Duffalo.

Per claim 18, Khorram teaches that an amplifier includes a plurality of transistors connected such that each amplifier has a common drain connection and a common gate connection (see figure 9, see abstract, column 10 and lines 60-column 11 and lines 25). Khorram does not teach wherein the drain of the first amplifier is connected to the gat of second amplifier.

Duffalo teaches such limitation (see figure 1 and items 44, 54 and 51). It would have been obvious to combine the references to properly supply DC bias current to the gate of the second amplifier.

Same arguments apply, *mutatis mutandis*, to claim 22 (obvious the terminals refer to the drain, gate and source, wherein the voltage applies on the gate control the current flow between the source and the drain)

Per claim 19, Duffalo further teaches the rain of the first amplifier is connected to the gate of the second amplifier through a capacitor (see figure 1item 41 and 51).

Same arguments apply, *mutatis mutandis*, to claim 23.

Per claim 20, Khorram further teaches that a first bias current (see figure 9 and item 220) connected to the common drain connection; a ground connected to the source of the first amplifier and the source of the second amplifier (see figure 9 and corresponding paragraphs). Kohorram does not teach a second bias current connected to the common gate connection. Duffalo teaches such limitation (see figure 1 and items 44, 54 and 51). It would have been obvious to combine the references to properly supply DC bias current to the gate of the second amplifier.

Same arguments apply, *mutatis mutandis*, to claim 24.

Per claim 21, Khorram further teaches a third amplifier including a source, a drain, and a gate (see figure 9 and item 228), wherein the gate of the third amplifier is connected to the

common gate connection, wherein the drain of the third amplifier is connected to the common drain connection. Kohorram does not teach a second bias current connected to the common gate connection. Duffalo teaches such limitation (see figure 1 and items 44, 54 and 51). It would have been obvious to combine the references to properly supply DC bias current to the gate of the second amplifier.

Same arguments apply, *mutatis mutandis*, to claim 25.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to YUWEN PAN whose telephone number is (571)272-7855. The examiner can normally be reached on 8-5 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Duc Nguyen can be reached on 571-272-7503. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Yuwen Pan/
Primary Examiner, Art Unit 2618